48. A semiconductor integrated circuit device according to claim 47, wherein each of said first conductor plugs comprises a multi-layer film of titanium nitride and tungsten.

49. A semiconductor integrated device according to claim 47, wherein said second conductor plug comprises a tungsten film. --

REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

This amendment is in response to the Office Action dated April 2, 2002. Appreciation is expressed to the Examiner, Mr. Pompey, for his courtesy and helpfulness during the personal interview conducted on July 11, 2002.

By the present amendment, claims 8-14 have been cancelled and new claims 42-49 have been added. These claims have been drafted to emphasize features which the Examiner indicated as appearing to overcome the cited reference to Chu (USP 5,783,471) during the above-noted interview (subject to the Examiner's further review of Chu and further search).

Briefly, the present new claims 42-49 are directed to an arrangement such as shown in the attached sketch, as well as features in forming such a structure shown, for example, in Figs. 8-13 of the specification. In particular, the present invention is directed to an arrangement using first and second insulating layers formed over a first portion used for a memory array and a second portion for circuits other than a memory array. More specifically, a plurality of first openings are simultaneously formed in the first insulating film over both the first and second portions, as shown in

Fig. 8. A plurality of first conductor plugs are then formed in the first openings, as shown in Fig. 9. Subsequently, as shown in Fig. 12, a second opening is formed in the second insulating film:

> "over an upper surface of one of the first conductor plugs formed in one of said first openings in the first insulating film and connected to the other of said first semiconductor regions of said MISFET." (as defined in new claims 42 and 47).

In this way, the first and second openings are respectfully formed in the first and second insulating films in such a manner that they can be very narrow and provide an excellent aspect ratio.

Reconsideration and allowance of new independent claims 42-47 and their dependent claims 43-46, 48 and 49 over Chu is respectfully requested.

Each of the independent claims 42 and 47 defines the feature of:

> "a plurality of first openings formed simultaneously in said first insulating film above both said first and second portions."

In conjunction with this, each of these claims defines a plurality of first conductor plugs formed within these first openings. In addition, claims 42 and 47 each define a second insulating film formed over the first insulating film and:

> "a second opening formed in said second insulating film over an upper surface of one of the first conductor plugs formed in one of said first openings in the first insulating film and connected to the other of said first semiconductor regions of said MISFET."

Claims 42 and 47 then define a second conductor plug formed in this second opening. As such, independent claims 42 and 47 clearly define the structure shown, for example, in the attached sketch, and excellent aspect ratios can be provided by virtue of the fact that the first openings are simultaneously formed in the first insulator, after which the first openings are filled with first conductor plugs, and then

the second opening is formed in the second insulator film over one of the first conductor plugs formed in one of the first openings.

As discussed during the interview, Chu is completely void of any suggestion of the claim structure. To begin with, Chu completely lacks the claimed feature of a second insulating film formed with a second conductive plug therein. Instead, Chu uses a single thick insulator BPSG 12 which is not at all analogous to the present claimed invention. In particular, the openings 333 for the conductor plugs 313 are formed in one step completely through the insulator 12. Therefore, the aspect ratio of these deep holes 333 will not be nearly as good as that which can be obtained in the two insulating film arrangement defined by the present claims 42-49.

It is also noted that there is no equivalent in the Chu reference for the claimed first openings formed simultaneously in the first insulating film above both the first and second portions. These differences were discussed during the interview, and Examiner Pompey agreed that these features appear to distinguish over the Chu reference. Accordingly, entry and allowance of new claims 42-49 over Chu is respectfully requested.

For the Examiner's convenience, a copy of a comparison table between claim 42 and the prior art to Chu is attached herewith. This comparison table shows distinctions discussed above as well as other differences of the present claimed invention over the Chu reference. As noted above, the Chu structure is quite different than that of the present claimed invention. By virtue of these differences, Chu is unable to obtain the excellent aspect ratios for the openings in the respective insulator layers. Therefore, consideration and allowance of claims 42-49 is respectfully requested.

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135 (501.35437CV2).

Respectfully submitted,

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【代理人提案クレーム】

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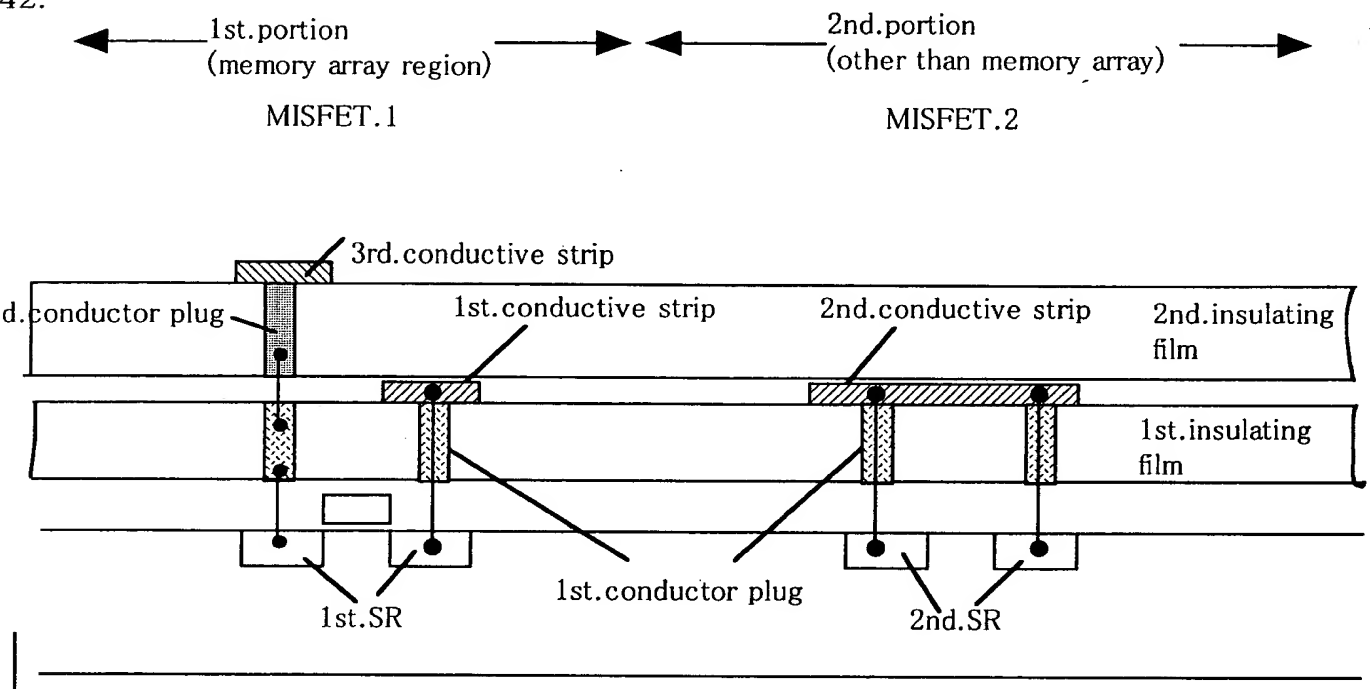

43. 1st. conductor plug : W

44. 1st. conductor plug : TiN/W

45. 2nd.SRs : P-type & N-type

46. 2nd.conductor plug : W

Comparison between claim 42 and prior art

	claim 42	prior art (USP5,783,471)	differences between claim 42 and prior art
memory array	1st.conductor plug	plugs (310A,310B)	
	1st.insulating film	insulating film (BPSG)	
	1st.conductor strip	-	
	2nd.conductor plug	plug (314,315)	2nd.conductor plug is formed in the 2nd.insulating film. Plug (314,315) is formed in insulating film (BPSG).
	2nd.insulating film	-	
	3rd.conductor strip	AL bit line (316)	3rd.conductor strip is formed on 2nd.insulating film. AL bit line(316) is formed on insulating film BPSG).
peripheral circuit	1st.conductor plug	plug (313)	1st.conductor plug in peripheral circuit is formed as the same step of forming the 1st.conductor plug in memory array rgion. Plug (313) is formed as the same step of plug (314,315).
	2nd.conductor strip	wiring (317)	

In claim 42, each plug is formed in each inter-layer insulating film, for exmple, a first plug is formed in a first insulating film and a second plug is formed in a second insulating film.

Therefore aspect ration of connecting hole is not so large in comparison to the prior art. Assuming that an insulating film (BPSG) includes the first and second insulating film of claim 42, the aspect ration of connecting hole formed plug (313) is large, because such connecting hole is formed in two layer of interlayer insulating film.